REMARKS

Claims 1-17 are presently pending. Claims 1-15 stand rejected. Claims 16 and 17 are added.

Claims 1-4 and 8-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Linzer.

Claims 5 and 13 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Ju.

Claims 6, 7, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Lavelle.

Additionally, Examiner objected to claim 9. Claim 9 is amended, and it is believed that claim 9 overcomes Examiner's objection.

With regards to claim 1 recites, among other limitations, "storing data in a machine readable memory device a first time at a first memory address;" and "storing the data in the machine readable memory device a second time at a second memory address".

Examiner has indicated that Linzer discloses "storing data in a machine readable memory devices (interpreted as any RAM) at a first time at a first memory address (pg. [0007], lines 3-6);" and "storing the data in the machine readable memory device a second time at a second memory address … (pg. 4, [0040], lines 1-6)."

Assignee respectfully notes that the citation, [0007], lines 3-6, refers to the "Summary of the Invention", while the alleged "storing the data in the machine readable memory device a second time at a second memory address", (pg. 4, [0040], lines 1-6), refers to the "Detailed Description of Preferred Embodiments".

It is respectfully submitted that one skilled in the art would not consider the teaching at [0007], lines 3-6 and [0040], lines 1-6 as cumulative, rather, that the "Summary of the Invention" would summarize "the invention" (In Linzer), of which Figures 4-7A, 7B are "Preferred Embodiments". Thus, Linzer does not teach or fairly suggest, "storing data in a machine readable memory device at a first time at a first memory address" and "storing the data in the machine readable memory device a second time at a second memory address".

Moreover, even if the "Summary of the Invention" and the "Detailed Description of Preferred Embodiments" were to be considered cumulative, Assignee respectfully submits that there is no teaching that the alleged, "storing data in a machine readable memory device a first time at a first memory address" at [0007], lines 3-6, is describing the "system 100", or "memory block 102" of FIGURES 4-7A, 7B in the "Detailed Description of the Preferred Embodiments". Thus, it is respectfully submitted that Lenzer does not teach "A method … comprising" "storing data in a machine readable memory device a first time at a first memory address;" and "storing the data in the machine readable memory device a second time at a second memory address".

Accordingly, for this reason, alone, Assignee respectfully traverses the rejection to claim 1, and dependent claims 2-8 and requests that Examiner withdraw it.

Additionally, claim 1 recites, "the first memory address having a first alignment with respect to the burst boundaries; ... the second memory address having a second alignment with respect to the burst boundaries." Examiner has indicated that Linzer teaches "a first alignment with

respect to the burst boundaries (pg. 4, [0033], lines 12-14); ... the second address having a second alignment with respect to the burst boundaries" (pg. 4, [0040], lines 1-6).

Linzer, pg. 4, [0033], lines 12-14 merely recites that "A 2-cycle burst generally provides a 2x8 region from one field (e.g., 2 byte aligned vertically, 8 byte aligned horizontally. In two such bursts, a 2x16 region from one field (e.g., 2-byte aligned vertically, 8-byte aligned horizontally) may be obtained that may cover any 9 pixels horizontally."

It is respectfully submitted that the foregoing does not teach "the second memory address having a second alignment with respect to the burst boundaries". The foregoing does not even teach "a second address", nor its particular "alignment with respect to the burst boundaries", much less "storing the data in the machine readable memory device a second time at a second memory address, the second memory address having a second alignment with respect to the burst boundaries". Accordingly, for the foregoing reason, Assignee respectfully traverse the rejection to claim 1, and dependent claims 2-8 and request that Examiner withdraw it.

Claim 9 recites, among other limitations "the set of desired bytes of data having been previously stored in a machine readable memory device at two or more memory addresses, the memory device having at least one burst boundary, and each memory address having a different alignment with respect to the at least one burst boundary" and Assignee traverse the rejection to claim 9 for at least the reasons above.

Additionally, claim 9 recites, “retrieving the desired bytes of data from a preferred memory address, the preferred memory address being aligned with the at least one burst boundary such that the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses”. Examiner indicates that the foregoing limitations is described at Linzer, p. 8, [0061], lines 1-10. Linzer [0061], merely describes “an example access pattern for a line mode in accordance with the present invention.” Linzer, [0061], lines 1-3. The foregoing has no teaching that “the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses”. Accordingly, for at least this reason as well, Assignee respectfully traverses the rejection of claim 9, and dependent claims 10-15 and requests that Examiner withdraw it.

Claim 16 is added and Assignee respectfully submits that claim 16 is allowable for at least the reasons indicated above. Additionally, claim 16 recites, “a circuit for writing the data to the machine readable memory device a first time starting at the first memory address that has the first alignment with respect to the burst boundaries and writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries”.

Although Examiner has indicated that Linzer teaches teaches “storing data in a machine readable memory devices (interpreted as any RAM) at a first time at a first memory

address (pg. [0007], lines 3-6);" and "storing the data in the machine readable memory device a second time at a second memory address … (pg. 4, [0040], lines 1-6).", it is respectfully submitted that Linzer, including the foregoing citations, also does not teach "writing the data to the machine readable memory device a first time" and "writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries".

Additionally, although Examiner has indicated that Linzer teaches "a first alignment with respect to the burst boundaries (pg. 4, [0033], lines 12-14); ... the second address having a second alignment with respect to the burst boundaries (pg. 4, [0040], lines 1-6)", it is respectfully submitted Linzer does not teach "starting at the first memory address" and "writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries." Accordingly, Examiner is respectfully requested to allow claim 16.

Claim 17 is added and recites, among other limitations,. "a machine readable memory device for storing data starting at a first memory address that has a first alignment with respect to burst boundaries, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries". Claim 17 is allowable for at least the reasons indicated with respect to claim 9.

Additionally, claim 17 recites, among other limitations, "a circuit for determining a first number of bursts for retrieving the data from the first address and determining a second number of bursts for retrieving the

data from the second address and retrieving the data from the first address if the first number of bursts is fewer than the second number, and retrieving the data from the second address if the second number of bursts is fewer than the first number".

Although Examiner has indicated that Linzer describes "retrieving the desired bytes of data from a preferred memory address, the preferred memory address being aligned with the at least one burst boundary such that the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses (pg. 8, [0061], lines 1-10)", it is respectfully submitted that Linzer does not teach "determining a first number of bursts for retrieving the data from the first address and determining a second number of bursts for retrieving the data from the second address". Accordingly, for at least this additional reason, Assignee submits that claim 17 is allowable.

Conclusion

For at least the foregoing reasons, Assignee respectfully submits that the application is in a condition for allowance and a notice of allowance is respectfully submitted.

The Commissioner is hereby authorized to charge any fees in connection with any of the actions requested herein to deposit account number 13-0017.

RESPECTFULLY SUBMITTED

May 29, 2007

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